U.G. 1st Semester Examination - 2020

COMPUTER SCIENCE

[HONOURS]

Course Code : Com.Sc-H-CC-L-T-102

(Digital System Design)

Full Marks : 60 Time : $2\frac{1}{2}$ Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP-A

1. Answer any **ten** questions: 2×10=20

   a) What are the advantages and disadvantages of synchronous over asynchronous counter?

   b) What do you mean by parity check?

   c) Write the truth table of 4:1 Mux.

   d) Simplify $F = AB + (AC)' + AB'C(AB + C)$.

   e) Implement two-input NOR function using NAND gates.

   f) Why D/A converter is useful?

   g) What are the limitations of the Karnaugh Map?

   h) Define setup time.

   i) State the advantages of edge triggering.

   j) State the excitation table of J-K flip-flop.

   k) Write the applications of shift registers.

   l) What is meant by tri-state logic?

   m) Differentiate between level triggering and edge triggering.

   n) Mention the classification of Integrated Circuits.

   o) Define noise margin.

GROUP-B

Answer any **four** questions: 5×4=20

2. How will you build a 16-input MUX using only 4-input MUX? Draw and explain.

3. Explain the working of 3-bit Synchronous up counter with necessary waveform and truth table.

4. Explain the working of positive edge-triggered D flip-flop with the help of a logic diagram.

5. a) Design an octal to binary encoder circuit with proper explanation.

   b) What is Fan out? 4+1

6. Implement the following functions:

$$F(A,B,C,D) = \Sigma m(1,4,8,13)$$

$$F(A,B,C,D) = \Sigma m(2,8,14,15)$$

using two 74183 (3 to 8) decoders.

7. Explain the working principle of 7477 BCD to 7-segment LED decoder.

GROUP-C

Answer any **two** questions: 10×2=20

8. a) Design a Combinational circuit to output the 2's complement of a 4-bit binary number.

   b) Design a full adder using 2-input NAND gates only. 6+4

9. a) Design a logic circuit that has 4 inputs, the output will only be high when at least two adjacent bits are same.

   b) Implement the function

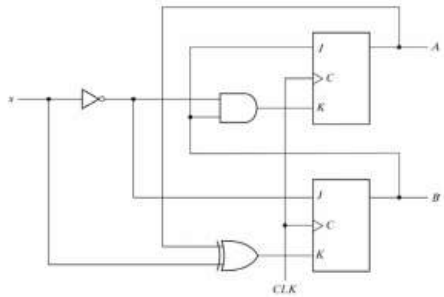
$$F(A, B, C) = \Sigma(1, 2, 5, 7)$$

   using 4 to 1 MUX. 6+4

10. a) Explain the working principle of 4-bit binary ripple counter with the help of logic diagram and truth table.

   b) Design a 3-bit even parity generator circuit. 6+4

11. a) Analyse the following sequential circuit and obtain excitation, transition and state tables. Draw the state transition diagram for the same.



   b) Define race condition. 8+2

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