U.G. 1st Semester Examination - 2019
COMPUTER SCIENCE
[HONOURS]
Course Code : Com.Sc(H)CCL-102-T

Full Marks : 60   Time : $2\frac{1}{2}$ Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP-A

1. Answer any **ten** questions: 2×10=20

    a) What is Duty cycle?

    b) Write the difference between Latch and Flip-Flop.

    c) Define Gray code.

    d) Why D/A converter is useful?

    e) Simplify F=BC+BC'+BA

    f) Write down the significance of preset input in flip-flop.

    g) State Consensus Law of Boolean algebra.

    h) Define LSI.

[Turn over]

i) Why encoders are useful?

j) State the excitation table of S-R flip-flop.

k) Expand $F=x+y\,z$ into minterms.

l) What do you mean by edge triggering?

m) Why NOR is called universal gate?

n) Why any Boolean function can be designed by using decoder?

o) How XOR can be used as NOT gate?

GROUP-B

Answer any **four** questions: $5\times4=20$

2. Draw and explain 3-input AND gate using Diode.

3. Design and implement Full subtractor using full adder.

4. a) Implement, with a decoder and external OR gates, the combinational circuit specified by the following two Boolean functions

   i) $f2(A, B, C) = \Sigma m(1, 2, 7)$

   ii) $f3(A, B, C) = \Pi M(0, 1, 2, 4)$

   b) What is Fan out?

                                                    $(2+2)+1$

5. Implement the following function using 8:1 MUX along with explanation

$$F(A, B, C, D) = \Sigma m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$$

6. Explain the working principle of J-K master slave flip-flop with circuit diagram along with waveform.

7. Design a three input A, B, C and one output Y circuit; minimal, two level gate combinational circuit which has an output equal to 'zero' when majority of its input are at logic '1'.


GROUP-C

Answer any **two** questions: 10×2=20

8. a) Convert D flip-flop to J-K flip-flop.

    b) Design a 1-bit comparator using 2-4 decoder giving 3 outputs G, E, L.   6+4

9. a) Explain race around condition.

    b) Design and describe asynchronous Decade Counter using J-K flip-flop. Draw the timing diagram also.   2+(6+2)

10. a) Write a short note on parallel adder.

   b) Simplify the following function. Also find out prime implicants and essential prime implicants:

   $$F(W, X, Y, Z) = \Sigma m(2, 3, 5, 7, 10, 11, 13, 14, 15)$$

   $$4+(4+1+1)$$

11. a) What will be the expression of Y for the following diagram.
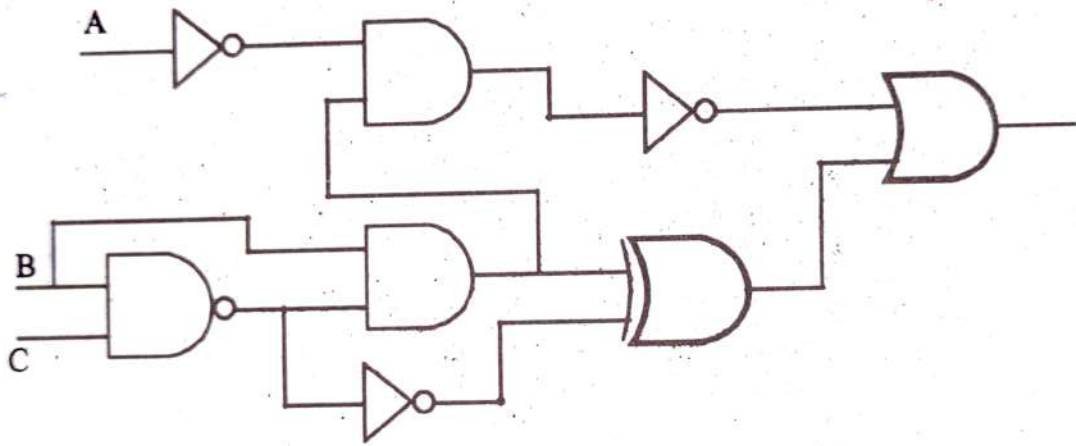
   Also draw the truth table for the same.

   b) Using a suitable decoder, design a circuit which will detect even no. of 1's in a 4-bit binary number. $(2+3)+5$